REMARKS

The present preliminary amendment is intended to address issues raised in the Official Action mailed October 25, 1999 in the parent case. In regards to applicant's amendment, claim 28 has been amended to clarify that what is being claimed is the embodiment as shown in Figures 10 and 11. Claim 28 has been amended to clarify that the dielectric material does not cover the edges of the inner dielectric layer after the vias are formed. The Examiner's indication in the interview summary of May 22, 2000 that it appears that the proposed amendment to claim 28 would overcome the primary reference to *Gall et al.* is appreciated.

In the parent case, claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34 were rejected under 35 U.S.C. § 103 as being unpatentable over *Gall et al.* (U.S. Patent 5,659,951) in view of *DiStefano et al.* (U.S. Patent 5,282,312). This rejection should not be repeated in the present case. The Examiner in the Office Action dated October 25, 1999 indicated that the patent to *Gall et al.* discloses a method of making a multi-layer circuit assembly including: providing an inner dielectric element 30e; providing first and second metal layers 26b, 26c; coating the inner dielectric layer and first and second metal layers with first and second outer dielectric layers 30d, 30g; forming one through vias 65 through the coated structure; providing a first outer metal layer 24b over the first outer dielectric layer 30d and a second outer metal layer 24d under the second outer dielectric layer 30g; and metalizing the coated through vias to form liners 40. The Examiner acknowledged, however, that *Gall* does not disclose that the dielectric material is formed by coating to form a coated structure.

The Examiner in the parent case alleged that *DiStefano et al.* teaches disposing flowable dielectric material by coating to form sheetlike layers of material for electrical circuit assemblies. The Examiner has indicated that this teaching is disclosed in col. 7, lines 29-47 of *DiStefano et al.* The Examiner's motivation to combine the *Gall et al.* reference and *DiStefano et al.* references in the parent case was that one of ordinary skill in the art at the time the invention was made would have known to modify the invention disclosed by *Gall et al.* by coating the dielectric material and the dielectric element to form sheetlike laminated layers of material for electric circuit assemblies, as disclosed by *DiStefano et al.*

However, the Office Action in the parent case did not allege that *DiStefano et al.* teaches applicant's step of forming dielectric layers and a dielectric liner in the vias, as claim 1 now requires. In claim 1, the recited process includes coating the metal layers and the through vias with a dielectric, then providing outer metal layers over said first and second outer dielectric layers, and metalizing said coated through vias to form metallic via liners connecting said outer metal layers. The metal via liners are separated from the first and second metal layers by the dielectric. Thus, the via liners are insulated from the first and second metal layers, except where an external connection is provided. With respect to claim 28 and its dependent claims, neither *Gall et al.* nor *DiStefano et al.* disclose coating an inner dielectric element and first and second metal layers with a dielectric material to form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively, as claim 28 requires.

A review of *Gall et al.* and *DiStefano et al.* reveals that they do not disclose all the limitations set forth in claims 1 and 28. As noted above, the Examiner in the parent case relied upon col. 7, lines 29-47 of *DiStefano et al.* in his rejection of claims 1 and 28. As shown in FIG. 5 for example, *DiStefano et al.* discloses a method of making multi-layer circuit assemblies utilizing a plurality of circuit panels 10 and interposers 12. Each interposer is disposed between two circuit panels. Each interposer has a flowable dielectric material on its major surfaces except at its interconnect locations. During the lamination process, some of the flowable dielectric material is forced into the vias. While the cited passage of *DiStefano et al.* discloses that dielectric material collects in reservoirs formed in via holes, *DiStefano et al.* does not disclose that the dielectric material lines the via holes, nor does it suggest subsequently depositing a metal layer in the through vias over the dielectric liner, as claim 1 requires. The art cited by the Examiner does not suggest that one would deposit a metal layer on any such dielectric material. Indeed, because the dielectric material referred to in this passage of the reference only enters the inside of the via liners during the lamination process, it is not seen how one could metalize the through via after that dielectric material is forced into the interior of the via liners. Further, the dielectric layer formed between the circuit panels and the interposer does not coat an inner dielectric element, as claim 28 requires. Accordingly, the combination of the *Gall et al.* reference and *DiStefano et al.* cannot render any of the previously rejected claims obvious.

Accordingly, since *Gall et al.* and *DiStefano et al.* do not render claims 1 or 28 obvious, they do no make any of the

claims that depend upon claims 1 and 28 obvious. For the reasons set forth above, the 103 rejection should not be repeated with respect to claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34.

The Examiner next rejected claims 6 and 31 in the parent case under 35 U.S.C. § 103(a) as being unpatentable over *Gall et al.* in view of *DiStefano et al.*, as applied to claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34 and further in view of *Tamm et al.* (U.S. Patent 5,666,722). As noted above, neither *Gall et al.* nor *DiStefano et al.* combined teach all of the limitations of the claims recited above. The Examiner applied the *Tamm et al.* reference in the parent case to teach metalizing the blind vias and through vias simultaneously. However, *Tamm et al.* also has not been asserted as teaching the limitations missing from *Gall et al.* in view of *DiStefano et al.* as previously discussed. Accordingly, the combination of the inventions disclosed by *Gall et al.*, *DiStefano et al.* and *Tamm et al.* does not render any of applicant's claims obvious.

The Examiner next rejected claim 11 in the parent case under 35 U.S.C. § 103(a) as being unpatentable over *Gall et al.* in view of *DiStefano et al.* as applied to claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34 above, and further in view of *Brauer et al.* (U.S. Patent 5,153,986). As previously stated, the combination of *Gall et al.* and *DiStefano et al.* does not teach all of applicant's claimed limitations as set out in claims 1 and 28. The Examiner has previously applied the *Brauer et al.* reference to teach depositing a seed layer over the first outer dielectric layer and under the second dielectric layer including the first and second metal layers.

However, the *Brauer et al.* patent has not been asserted as teaching the limitations missing from the *Gall et al.* reference. Accordingly, the combination of the inventions disclosed by *Gall et al.*, *DiStefano et al.* and *Brauer et al.* cannot render any of applicant's claims obvious.

The Examiner next rejected claims 16, 18, 26 and 27 in the parent case under 35 U.S.C. § 103(a) as being unpatentable over *Gall et al.* The Examiner indicated that it would have been an obvious design choice to choose any desired dimension of thickness for the dielectric material, diameter of through vias and first and second metal layers since applicant has not disclosed that the claimed dimension of thickness solves any stated problem. It is applicant's assumption that since claim 1 was rejected under *Gall et al.* in view of *DiStefano et al.*, it was the Examiner's intention to reject claims 16, 18, 26 and 27 under *Gall et al.* in view of *DiStefano et al.* Again, since *Gall et al.* and *DiStefano et al.* fail to disclose all of applicant's claimed limitations in claims 1 and 28, the combination of *Gall et al.* and *DiStefano et al.* cannot make obvious any of applicant's dependent claims. Also, it is not clear on this accord as to whether *Gall et al.'s* drilling process would be practiced with a 200 micron (.0078") diameter hole, to yield an insulated hole of 150 microns (.006"), as recited in claim 18, one would need a .006 inch drill and the ability to place such a drill and keep it on a straight path through the multiple layers.

As it is believed that all rejections and requirements set forth in the Official Action dated October 25, 1999 in the parent case have been fully met by the foregoing preliminary amendment and remarks, favorable reconsideration and allowance of the application are earnestly solicited.

If there are any additional charges in connection with this Preliminary Amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor. If the Examiner has any questions, we respectfully ask that the Examiner contact the undersigned at the address, telephone and facsimile information set forth below.

Respectfully submitted,

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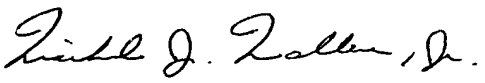

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